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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,665	08/31/2001	Toshiharu Furukawa	BUR919990305US1	3799

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EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/944,665	Applicant(s) FURUKAWA ET AL.	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 18-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. Applicant's election with traverse of claims 18-44 in Paper No. 8 is acknowledged. The traversal is on the ground(s) that the restriction requirement is improperly based on the drawings and the Examiner has not articulated a sufficient reason to insist on the restriction. The Examiner agreed with the applicants and withdrawn the species restriction which is based on the drawings. The Examiner will also examine claims 1-10. However, the Examiner is still maintained the restriction requirement, which is based on the device claims and the method claims. The arguments of the applicants are not persuasive because the device claims and the method claims are independent and distinct from each other. Each of the device claims and method claims would require separate search and examination.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 11-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 8.

3. The disclosure is objected to because of the following informalities:

In page 9, line 29, change "ande" to "and".

There is no reference numeral 1530 (page 12, line 23) in figs. 15A to 15C.

Appropriate correction is required.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 3, lines 3-5, the phrase "a contact formed in an

opening in said isolation material adjacent said insulating material to a conductive region at an end of said pillar". Claim 23, lines 2-3, the phrase "said gate structure extends on at least three sides of said channel". Claim 33, lines 5-8, the phrase "said contact between said first diffusion and said another diffusion extends over insulation between said first transistor and said second transistor". Claim 34, lines 2-3, the phrase "said insulation comprises an etched and deposited isolation structure". Claim 35, lines 2-4, the phrase "said substrate comprises SOI having buried oxide isolation and wherein said insulation comprises said buried oxide isolation". Claim 37, lines 2-4, the phrase "said gate structure comprises a continuous interior wall entirely surrounding said channel and spaced therefrom by a dielectric layer". Claim 38, line 2, the phrase "said gate structure is self-aligned to said channel". Claim 41, lines 5-6, the phrase "a borderless opening at least through a portion of the dielectric material on said top surface".

5. Claims 2, 3, 6, 8, 20 and 35 are objected to because of the following informalities:

Claim 2, lines 2-3, the phrase "said layer of insulating material" is unclear whether it is being referred to "said layer of insulator".

Claim 3, line 4, the phrase "said insulating material" has no antecedent basis.

Claim 6, line 7, the phrase "said trenches" has no antecedent basis.

Claim 8, lines 4-5, the phrase "said insulating material" has no antecedent basis.

Claim 20, line 2, the phrase "said gate" has no antecedent basis.

Claim 35, line 2, the phrase "SOI" should be in full word form instead of in abbreviation; line 3, "said insulation" has no antecedent basis.

Appropriate correction is required.

6. Claims 1-10 and 18-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 10-13, the phrase "said insulator material being selectively etchable relative to said sidewalls and said semiconductor pillar" is unclear whether the insulator material has been etched to form a contact opening adjacent to the sidewalls and the semiconductor pillar.

Claim 2, lines 4-6, the phrase "said isolation material being selectively etchable relative to said layer of insulator" is unclear whether the isolation material has been etched to form a contact opening adjacent to the layer of insulator.

Claim 6, lines 9-11, the phrase "said isolation material being selectively etchable relative to said layer of insulator" is unclear whether the isolation material has been etched to form a contact opening adjacent to the layer of insulator material.

Claim 18, line 9, the term "borderless" is unclear whether a contact to said first diffusion extends over the top surface of the gate structure.

Claim 24, line 3, the term "borderless" is unclear whether a contact to the second diffusion extends over the top surface of the gate structure.

Claim 29, line 2, the phrase "said gate structure is borderless to said second diffusion" is unclear as to how the gate structure is borderless to the second diffusion. Figs. 23C and 37C shows the gate structure is border to the second diffusion.

Since a spacer is different from the contact, it is unclear how the contact to said second diffusion comprises a spacer self-aligned to said edge in claim 30.

Claim 40, line 2, the phrase "sub-lithographic width" is unclear as to what is the actual width of the channel.

Claim 41, line 5, the term "borderless" is unclear whether a contact opening to the first diffusion extends over the top surface of the gate structure.

Claim 42, line 5, the term "borderless" is unclear whether a contact opening to the second diffusion extends over the top surface of the gate structure.

Claim 43, line 5, the term "borderless" is unclear whether a contact opening to the gate structure extends over the top surfaces of the first and second diffusions.

Claim 44, line 3, the term "borderless" is unclear whether it is being referred to the contact opening as mentioned in the rejection of each of claims 41, 42 and 43.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Alavi et al.

In regards to claim 1, Alavi et al. shows all the elements of the claimed invention in figs. 1-43. It is a vertical field effect transistor, including: a semiconductor pillar conduction channel (n-Si), gate electrodes (POLY) [30] in trenches adjacent the semiconductor pillar [22, 24, 20], a layer of insulator (ILD) [44] adjacent the gate electrodes and opposite said semiconductor pillar, sidewalls (OXIDE) adjacent said semiconductor pillar above said gate electrodes in said trenches, insulator material [44] in said trenches above said gate electrodes and adjacent said sidewalls, said insulator material [44] being selectively etchable relative to said sidewalls and said semiconductor pillar.

In regards to claim 2, Alavi et al. further discloses isolation material [44] (outermost portion of layer [44]) adjacent said layer of insulator and surrounding said vertical transistor, said isolation material being selectively etchable relative to said layer of insulator.

In regards to claim 3, Alavi et al. further discloses a contact [S] formed in an opening in said isolation material adjacent said insulator material to a conductive region [12] at an end of said pillar.

In regards to claim 4, Alavi et al. further discloses a contact [D] formed in an opening to an end of said pillar, and a contact [G1] formed an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall (sidewall spacer) [41] on said pillar.

In regards to claim 5, Alavi et al. further discloses a spacer [14] in said trench between said gate structure and a bottom of said trench.

In regards to claim 6, Alavi et al. shows all the elements of the claimed invention in figs. 1-43. It is an integrated circuit device, including: isolation material [44] surrounding transistor locations in a substrate [12], vertical field effect transistors [60] formed at said transistor locations and having a gate electrode structure (POLY) [30] formed in a trench, a layer of insulator material (ILD) in said trenches between said isolation material [44] (outermost portion of layer [44]) and said gate electrode structure, said isolation material being selectively etchable relative to said layer of insulator material, and a contact opening [S] formed along an interface of said layer of insulator material and said isolation material.

In regards to claim 7, Alavi et al. shows said gate electrode structure includes dual gate electrodes extending on opposite sides of a conduction channel (n-Si).

In regards to claim 8, Alavi et al. shows a contact [S] formed in said contact opening in said isolation material adjacent said insulator material and extending to a conductive region [12] extending below said pillar.

In regards to claim 9, Alavi et al. shows a contact [D] formed in an opening to an end of said pillar, and a contact [G1] formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall [41] on said pillar.

In regards to claim 10, Alavi et al. shows a spacer [14] in said trench between said gate structure and a bottom of said trench.

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 18, 19, 32, 38, 39 and 40 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Malhi et al.

In regards to claim 18, Malhi et al. shows all the elements of the claimed invention in figs. 7A-7C and 9. It is a transistor, comprising: a substrate [106', 108], a first diffusion [16"], a second diffusion (n+) above said first diffusion, a channel (p) [20] extending vertically between said first diffusion and said second diffusion, a gate structure extending on at least one side of said channel, and a contact (OUTPUT) to said first diffusion borderless to said gate structure.

In regards to claim 19, Malhi et al. shows the transistor is a vertical transistor and wherein said first diffusion [16"] is formed in said substrate and said second diffusion is formed on said channel.

In regards to claim 32, Malhi et al. shows an isolation structure [112], wherein the transistor is self-aligned to said isolation structure.

In regards to claim 38, Malhi et al. shows the gate structure is self-aligned to said channel.

In regards to claim 39, Malhi et al. shows the first diffusion [16"] comprises a dopant species provided separately from said second diffusion.

In regards to claim 40, Malhi et al. shows the channel has a width.

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 25 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malhi et al.

In regards to claim 25, Malhi et al. shows the transistor comprises a pillar of silicon having an edge. Malhi et al. differs from the claimed invention by not showing the silicon is a single crystal silicon. It would have been obvious for the silicon is a single crystal silicon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

In regards to claim 35, Malhi et al. shows the substrate comprises SOI (silicon-on-insulator) having buried isolation [102]. Malhi et al. differs from the claimed invention by not showing the isolation is an oxide isolation. It would have been obvious for the isolation is an oxide isolation, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

13. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malhi et al. in view of Alavi et al.

In regards to claim 26, Malhi et al. shows the pillar comprises the channel and the second diffusion, and the gate structure extending adjacent the pillar.

Malhi et al. differs from the claimed invention by not showing the pillar comprises the first diffusion.

Alavi et al. shows the pillar comprises the first diffusion (p+) in fig. 39.

Since both Malhi et al. and Alavi et al. show a vertical transistor having a pillar, it would have been obvious to have the first diffusion of Alavi et al. in Malhi et al. because it depends on the speed of the device.

In regards to claim 27, Malhi et al. shows the first diffusion [16"] extends into the silicon beneath the pillar and extends below the gate structure for formation of a contact adjacent the gate structure. Malhi et al. differs from the claimed invention by not showing the silicon is a single crystal silicon. It would have been obvious for the silicon is a single crystal silicon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

In regards to claim 28, Malhi et al. shows an insulator adjacent the gate structure, wherein the contact to the first diffusion comprises a conductive layer adjacent the insulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

si
October 20, 2002

Steven Loke
Primary Examiner